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L4: Entry 1 of 1 File: USPT Oct 18, 1983

DOCUMENT-IDENTIFIER: US 4410943 A
TITLE: Memory delay start apparatus for a queued memory controller

CLAIMS:

5. The controller of claim 2 wherein said queue control means includes:

at least one bistable indicator means, said bistable indicator means being coupled to said queue circuit means and to said bus, said bistable indicator means being switched from a first to a second state in response to each of said number of requests being stored in said queue circuit means and wherein said memory delay start control means further includes:

logic gating means coupled to said timing generator means, to said delay circuit means, to said queue control means and to said recycle control means, said logic gating means being operative to generate delay start timing signals by logically combining said control signals and said availability status signals, said recycle control means being conditioned by each of said delay start timing signals to initiate said successive memory cycles of operation within said minimum period of time.

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L8: Entry 1 of 4 File: USPT May 31, 1994

DOCUMENT-IDENTIFIER: US 5317701 A

**** See image for Certificate of Correction ****

TITLE: Method for refilling instruction queue by reading predetermined number of instruction words comprising one or more instructions and determining the actual number of instruction words used

Detailed Description Text (9):

In the present invention, prefetch controller 56 is operable in two modes, a sequential mode, and a change of flow mode. When operating in the sequential mode, prefetch controller 56 alternates the loading of QUEUE ZERO 51a and QUEUE ONE 51b, as previously described. Essentially, in the sequential mode of operation, prefetch controller 56 issues a memory READ REQUEST signal based upon the number of words remaining in the instruction queue 50, after loading the INU 32. In contrast, when operating in the change of flow mode, prefetch controller 56 loads both QUEUE ZERO 51a and QUEUE ONE 51b from the instruction cache 38 (or external memory 22), irrespective of the number of words remaining in the instruction queue 50. Thus, once INU 32 determines that the resident instruction is a change of flow (COF) instruction, INU 32 sends a COF signal to the prefetch controller 56. In response to the COF signal, prefetch controller 56 loads QUEUE ZERO 51a, for example, and loads QUEUE ONE 51b, immediately following the loading of QUEUE ZERO 51a. These prefetches place the instruction queue 50 in the same state as if the target instruction (e.g. branch) was reached through in-line instruction execution.

L11: Entry 1 of 8 File: USPT Jan 18, 2005

DOCUMENT-IDENTIFIER: US 6845472 B2
TITLE: Memory sub-system error cleansing

CLAIMS:

39. A system for correcting errors detected in a memory device, the system comprising: a memory sub-system comprising: a plurality of memory cartridges configured to store data words; a cleansing device configured to periodically initiate an internal READ command to the plurality of memory cartridges in response to an event, the internal READ command being issued to the plurality of memory cartridges on a memory network bus; and a monitoring device configured to monitor the memory network bus and further configured to change the frequency of periodic initiations of the internal READ commands based on the number of requests on the memory network bus over a period of time; and a host controller operably coupled to the memory sub-system and comprising: an arbiter configured to schedule accesses to the memory sub-system; error detection logic configured to detect errors in a data word which has been read from the plurality of memory cartridges; a memory engine configured to correct the errors detected in the data word which has been read from the plurality of memory cartridges in response to the internal READ command initiated by the cleansing device and configured to produce a corrected data word corresponding to the data word in which an error has been detected; scrubbing control logic configured to request a write-back to each memory location in which the error detection logic has detected an error in a data word which has been read from the memory sub-system; and one or more memory buffers configured to store the corrected data word.

L11: Entry 2 of 8 File: USPT May 11, 2004

DOCUMENT-IDENTIFIER: US 6735637 B2
TITLE: Method and system for providing advanced warning to a data stage device in order to decrease the time for a mirror split operation without starving host I/O request processsing

Detailed Description Text (23):
Although the present invention has been described in terms of a particular embodiment, it is not intended that the invention be limited to this embodiment. Modifications within the spirit of the invention will be apparent to those skilled in the art. For example, split advance warning techniques can be incorporated into any number of different types of data storage devices, including disk arrays, but in no way limited to disk arrays. As with any procedural technique, there are an almost limitless number of ways of implementing split advance warning, both in software as well as in firmware and hardware. In the above example, the WRITE processing ratio used to control the rate of local WRITE processing versus mirror WRITE processing is based on a maximum number of WRITE requests that can be processed each second by the disk-array controller on behalf of a mirror LUN. However, in more sophisticated systems, it may well be possible to calculate the actual time required for the different queued WRITE requests, and incorporate such calculations in determining the appropriate ratio of WRITE processing rates in order to achieve mirror data consistency between the LUNs of a mirror pair in the time between a split advance warning and issuance of a corresponding mirror split operation request. The technique employed in order to achieve data consistency may vary from a ratio-based technique, as described above, to other empirical or calculated methods that result in favoring mirror WRITE requests over host WRITE requests during the interval between the split advance warning and issuance of a mirror split operation. In the above-discussed example, the mirror LUN consists of a local LUN and a remote LUN but, as already discussed, the split advance warning technique is equally applicable to mirror LUNs within the same data storage device. Moreover, the split advance warning may be employed for mirroring techniques that involve more than two LUNs, such as a mirror triple, and that may be applied at a granularity different than a LUN granularity. For example, split advance warning might be employed in the aggregate for all pending host WRITE operations and pending mirror WRITE operations. As another example, processing of host-computer WRITE requests may slowed for all LUNs provided by a disk array in order to bring a particular mirror pair into a consistent state. As discussed above, the pseudocode implementation focused on processing WRITE requests, but other type of I/O requests that can change the state of a data storage device need also be included in the split advance warning technique.

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L11: Entry 3 of 8 File: USPT Apr 27, 2004

DOCUMENT-IDENTIFIER: US 6727803 B2
TITLE: Method and apparatus for efficiently querying and identifying multiple items on a communication channel

Detailed Description Text (24):
At step 104, assuming the length of the bit string is equal to K bits, the system pushes the current bit string to the isolated transponder stack, and continues to step 106. At step 106, the system initializes the current bit string buffer and proceeds to step 108. At step 108, the system determines if the non-isolated transponder stack is empty; if this criterion applies, then the system proceeds to step 78, where the system stops and the algorithm is completed; however, if this criterion does not apply, then the system proceeds to step 110. At step 10, the interrogating system pops the last entry from the non-isolated stack, and returns to step 74. As previously described, the CHANGE 1 command instructs the transponder to switch to the READ mode, whereupon the transponder will serially shift out the bits of its ID number in response to serial commands from the interrogating transceiver as illustrated in FIG. 6.

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L11: Entry 6 of 8 File: USPT Mar 31, 1981

DOCUMENT-IDENTIFIER: US 4259549 A
TITLE: Dialed number to function translator for telecommunications switching system control complex

CLAIMS:

23. In a microprocessor control means for a telephone switching system having switching network means supervised by network controller means providing sense and control point pair means for deriving and terminating information respectively, said microprocessor control means comprising first microprocessor means including first memory means and first interprocessor buffer means for monitoring said sense points, writing said control points and storing the current status for all lines, trunks and registers of the switching system and providing next states-of-call therefor, second microprocessor means including second memory means and second interprocessor buffer means for controlling a plurality of registers to accept and process dialing information, third microprocessor means including third memory means and third interprocessor buffer means for performing dialed number translations, and means for selectively interconnecting said interprocessor buffers to exchange data between said microprocessor means for controlling said telephone switching system; the improvement in said means for performing dialed number translations comprising: data base memory means for correlating system operational functions and dialed numbers including a plurality of addressed locations, each of said locations providing means for storing coded electrical signals representing an instruction designating a specific operational function, each of said locations having an address employing digits of a directory number and said third microprocessor means including means for addressing said data base memory means in response to a dialed directory number to retrieve a designated instruction, said third microprocessor means providing commands based on retrieved instructions to other of said microprocessor means, for controlling said switching system.